3-to-8 Decoder using VHDL (Hierarchical Design)

EE 3109 Computer Aided Digital Design

Lab Assignment #7

Due: November 02, 2007

The purpose of this exercise is to design and simulate a 3-to-8 Decoder using 2-to-4 Decoders. The 2-to-4 Decoder must be designed in the same way as explained in the class. Use the ALTERA QUATRUS II package to implement your circuits.

Step 1: Designing a 2-to-4 Decoder
1. Design a 2-to-4 decoder circuit using VHDL
2. Create a new project and label it as “decoder24”
3. 3 inputs and 4 outputs
   A2, A1, CS1: in std_logic;
   O1, O2, O3, O4 : out std_logic;
4. The library files that must be used before the start of the VHDL code is
   LIBRARY ieee;
   USE ieee.std_logic_1164.ALL;
   USE ieee.numeric_std.ALL;
5. CS1 (Chip Select/Enable) = 1, enables the decoder otherwise the decoder is disabled (Output = 0).
6. Verify your design by constructing the timing waveform.

Step 2: Designing a 3-to-8 Decoder
1. Use two 2-to-4 Decoders and added gate(s) to implement a 3-to-8 Decoder.
2. Create a new project and label it as “decoder38”
3. 4 inputs and 8 outputs
   B3, B2, B1, CS2: in std_logic;
   P1, P2, P3, P4, P5, P6, P7, P8: out std_logic;
4. CS2 = 1, enables the decoder otherwise the decoder is disabled (Output = 0). Note that this CS is different from the CS of 2-to-4 decoder.
5. Refer to page 270 in the book on how to use components.
6. Verify your design by constructing the timing waveform.

Step 3: Waveforms
Your report must include the following.
   a. VHDL code for 2-to-4 decoder
   b. Waveform for 2-to-4 decoder (8 possible combinations)
   c. VHDL code for 3-to-8 decoder
   d. Waveform for 3-to-8 decoder. (16 possible combinations)

Turn in the report before 5:00PM on the due date. Remember to write your report in the format that was given to you during the first class.