EE 3109 Computer Aided Digital Design
Lab Assignment # 8
Sequence Detector (Moore Machine) using VHDL

Due: November 9, 2007

The purpose of this exercise is to become familiar with the sequential architecture of VHDL by implementing and simulating a clocked sequential network machine using VHDL. Use ALTERA QUATRUS II for simulation.

I. Design your Moore machine as follows

1) The Moore machine has an input sequence X and an output sequence Z. The output (Z) becomes one when any input (X) sequence ends in 010.
   For Example:  \[ X = 0 \, 0 \, 0 \, 1 \, 0 \, 1 \, 0 \, 0 \, 0 \, 1 \, 1 \, 1 \, 0 \, 1 \, 0 \, 0 \]
   \[ Z = 0 \, 0 \, 0 \, 0 \, 1 \, 0 \, 1 \, 0 \, 0 \, 0 \, 0 \, 0 \, 0 \, 0 \, 1 \, 0 \]

2) Start your design by creating a state graph for your machine. Recall that the output in a Moore machine is linked to the state.
   a) You should create as many states as needed by your design.
   b) Make sure you take into account all transitions from one state to another.

II. Write your code using the following signals:

1) Inputs
   a) Clk
   b) Input (X)
   c)Reset

2) Outputs
   a) Output (Z)
   b) State (go to node finder and change options in filter section)

III. Your report should contain the following

1) The state graph
2) The VHDL Code
3) Two waveforms
   a) One in which you give a sequence of inputs and Reset is not active (Low).
   b) One in which Reset is active (High) at least in one of the states.

IV. Turn in the report before the start of the class. Remember to write your report in the format that was given to you during the first class.

Reading:
2. Class Notes

Pre-Lab

Due – Nov 7, 2007

A sequential network has one input (X) and one output (Z). An output \( Z = 1 \) occurs every time the input sequence 010 is completed. Derive a Moore state graph and state machine. Draw the circuit and show all the steps.