Lesson 11: Accumulator

Computer Aided Digital Design
EE 3109
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Fall 2007

Accumulator

CLOCK

data_in
regin/sum
data_out

RESET=1
Lab10

- 4 VHDL printouts
- 5 Waveforms

75 points.

One page description needed.

Demonstrations

- Last week for demonstrations

Extra Credit – worth 50 points

- Due Dec 07, 2007
- Email me and get confirmation.
- Not all labs are worth 50 points.
- Points are assigned on complexity of lab
- Can be VHDL or Schematic based.

Folio – Due Friday, Dec 05, 2007

- Final Labs
  - Lab1
  - Lab2
  - ...
  - Lab10
- Schematics/VHDL (.vhd, .bdf)
- Waveforms (.vwf)
- Reports

Exam 2 – Nov 30, 2007

- Topics
  - Multiplexers
    - 4 variable truth table (4 inputs, 1 output)
    - 8:1 mux implementation
  - Mealy Machine using J-K flipflops
    - Similar to lab8
  - VHDL Code
    - Modifications
  - Counter design using state table
    - 0,1,6,2,0
    - using 2 flip-flops